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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,752	11/26/2003	David Goren	IL920030043US1	9934

7590 07/27/2005

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,752	GOREN ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/26/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/18/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Responsive to communication application filed on 11/26/2003, claims 1-24 are pending.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "crossing line" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 1-24 are objected to because of the following informalities: these claims contain an element "crossing line", which is not in the drawings. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Alon et al. (Alon) (US 2003/0172358),

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

5. **With respect to claims 1-6, 11, 12-15, 20 and 21**, Alon discloses a method (pg. 1, ¶ 12), system (pg. 1, ¶ 17), and computer program product comprising a computer readable medium having embodied therein computer readable program code

(instruction) means for causing a computer implement (pg. 1, ¶ 22) for designing a integrated circuit comprising:

(**claims 1, 2, 12, 13, 21**) (means) defining a preliminary design (high level design) of the integrated circuit (fig. 1, step 12; fig. 2, step 22, and pg. 1, ¶ 12);

(**claims 1, 12, 21**) (means) identifying critical interconnect lines in the preliminary design (pg. 1, ¶ 13; pg. 2, ¶ 19 and ¶ 22);

(**claims 1, 3, 12, 14, 21**) (means) identifying any critical interconnect lines affected by crossing lines (cross/couple capacitance) in the preliminary design (pg. 1, ¶ 5 and ¶7);

(**claims 1, 12, 21**) (means) defining a transmission line model to represent each critical interconnect line (pg. 2, ¶14, ¶18; pg. 3, ¶ 33);

(**claims 1, 12, 21**) (means) defining a layout design of the integrated circuit, comprising circuit components and parameters thereof using said preliminary design and said transmission line model for each critical interconnect line (pg. 1, ¶ 13 and pg. 2, ¶ 18); and

(**claims 1, 11, 12, 20, 21**) (means) extracting component parameters from the layout design for simulation of the design using the extracted component parameters (pg. 1, ¶ 5, 13 and pg. 2, ¶ 18);

(**claims 1, 4-6 12, 15, 21**) wherein for each transmission line model representing a critical interconnect line affected by a crossing line (cross/couple capacitance) (pg. 1, ¶ 5 and ¶7), the method includes providing an environment terminal (pg. 2, ¶ 18 and ¶ 28), comprising a connection to the model via at least one circuit component representing the effect of the crossing line on the model (fig. 3a-3c) , and connecting the

environment terminal to the crossing line in the integrated circuit design (pg. 2-3, ¶ 31 and pg. 3, ¶ 37).

6. **With respect to claim 7,** Alon discloses a method according to claim 2 wherein the step of defining a layout design comprises:

defining a schematic design of the integrated circuit, comprising a preliminary set of circuit components and parameters thereof using said high level design (fig. 1, step 12; fig. 2, step 22, and pg. 1, ¶ 12, ¶ 13; pg. 2, ¶ 19 and ¶ 22) and said transmission line model for each critical interconnect line (pg. 2, ¶14); and

defining the layout design, comprising a secondary set of circuit components and parameters thereof and indicating component locations, using said schematic design (fig. 3 and pg. 5, ¶ 66-¶ 70).

7. **With respect to claims 8 and 17,** Alon discloses all the limitations according to claims 1 and 12, respectively, wherein the transmission line model defined for each critical interconnect line comprises an RLC network (pg. 4, ¶ 56).

8. **With respect to claims 9 and 18,** Alon discloses all the limitations according to claim 1 and 12, respectively, wherein the step of designing a transmission line model comprises:

defining a transmission line structure (pg. 2 and 3, ¶ 31, ¶ 33);

defining geometrical parameters for the transmission line structure (pg. 3, ¶ 45; pg. 5, ¶ 69); and

designing the transmission line model in dependence on said structure and geometrical parameters (pg. 3, ¶ 38, and pg. 4, ¶ 48-53; pg. 5, ¶ 69).

9. **With respect to claim 10 and 19,** Alon discloses all the limitations as the set rejection above, wherein the step of defining a transmission line structure comprises selecting the structure from a predefined set of transmission line structures (pg. 2, ¶ 14).

10. **With respect to claim 16,** Alon discloses system according to claim 12 wherein said means for including an environment terminal (cross/couple capacitance) in the design comprises said post-layout exaction means (pg. 1, ¶ 5 and ¶7).

11. **With respect to claim 22,** Alon discloses computer program product comprising a computer-readable medium having embodied therein computer-readable program code means for causing a computer to implement an interconnect modeling component of an integrated circuit design system, the interconnect modeling component being adapted for (pg. 2, ¶22):

defining transmission line models to represent respective critical interconnect lines in an integrated circuit design (pg. 2, ¶14, ¶18); and

providing, for a said transmission line model representing a critical interconnect line affected by a crossing line in the integrated circuit design (cross/couple capacitance) (pg. 1, ¶ 5 and ¶7), an environment terminal comprising a connection to the model via at least one circuit component representing the effect of said crossing line on the model (pg. 2, ¶ 18 and ¶ 28 and fig. 3a-3c).

12. **With respect to claim 23,** Alon discloses an integrated circuit design kit including a product according to claim 22 (pg. 2, ¶ 19, and ¶22).

13. **With respect to claim 24,** Alon discloses computer program product comprising a computer-readable medium having embodied therein computer-readable program code means for causing a computer to implement a post-layout extraction component of

an integrated circuit design system in which critical interconnect lines in an integrated circuit design are represented by respective transmission line models (pg. 2, ¶ 30), the post-layout extraction component being adapted for processing a layout design of the integrated circuit (pg. 3, ¶ 41-42), which layout design comprises circuit components, including said transmission line models, and parameters thereof (pg. 2, ¶ 22), by:

including in the layout design, for a transmission line model representing a critical interconnect line affected by a crossing line in the design (cross/couple capacitance) (pg. 1, ¶ 5 and ¶7), an environment terminal connected to said crossing line, the environment terminal comprising a connection to said model via at least one circuit component representing the effect of said crossing line on the model (pg. 2, ¶ 18 and ¶ 28 and fig. 3a-3c); and

extracting component parameters from the layout design for simulation of the design using the extracted component parameters (pg. 1, ¶ 5, 13 and pg. 2, ¶ 18).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nghia M. Doan
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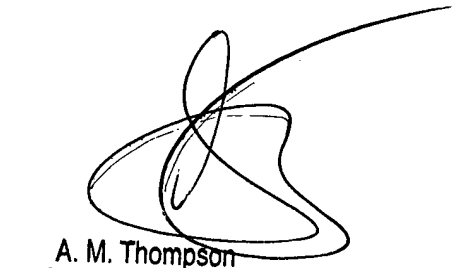
NMD



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